We claim:

1. A method for decoding a signal received from a dispersive channel causing intersymbol interference, said signal encoded using the MLT-3 code, said method comprising the steps of:

generating at least one trellis representing said MLT-3 code and said dispersive channel; and

performing joint equalization and decoding of said received signal using said trellis.

2. The method of claim 1, wherein said performing step uses a reduced complexity sequence estimation technique.

3. The method of claim 1, wherein said performing step uses the Viterbi algorithm.

4. The method of claim 1, wherein said generating step further comprises the step of concatenating a trellis representing said MLT-3 code and a trellis representing said dispersive channel.

5. The method of claim 1, wherein said MLT-3 code uses three signal levels to represent two binary values.

6. The method of claim 1, wherein said trellis representing said MLT-3 code has a plurality of trellis states, each of said trellis states associated with a value for a signal in a previous symbol period and each of said trellis states having at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values.

7. The method of claim 1, wherein said dispersive channel is an Ethernet channel.

8. A receiver for processing a signal received from a dispersive channel, said signal encoded using an MLT-3 code, comprising:

a sequence detector that performs joint equalization and decoding of said received signal using at least one trellis representing said MLT-3 code and said dispersive channel.

9. The receiver of claim 8, wherein said sequence detector employs a reduced complexity sequence estimator.

10. The receiver of claim 9, wherein said reduced complexity sequence estimator employs a reduced-state trellis having a reduced number of states, wherein said reduced complexity sequence estimator further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states;

a survivor memory unit (SMU) that stores said best surviving paths; and

a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis.

11. The receiver of claim 8, wherein said sequence detector employs the Viterbi algorithm.

12. The receiver of claim 11, wherein said sequence detector employs a super trellis that concatenates said trellis representing said MLT-3 code and said trellis representing said dispersive channel, wherein said sequence detector further comprises:

a branch metric units (BMU) that calculates branch metrics based on said received signal;

an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states; and

a survivor memory unit (SMU) that stores said best surviving paths.

13. The receiver of claim 8, wherein said at least one trellis is a concatenation of a trellis representing said MLT-3 code and a trellis representing said dispersive channel.

14. The receiver of claim 8, wherein said trellis representing said MLT-3 code has a plurality of trellis states, each of said trellis states associated with a value for a signal in a previous symbol period and each of said trellis states having at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values.

15. The receiver of claim 8, wherein said dispersive channel is an Ethernet channel.

16. A method for representing an MLT-3 code as a trellis, said MLT-3 code using three signal levels to represent two binary values, said method comprising the steps of:

generating said trellis with a plurality of trellis states, each of said trellis states associated with a value for a signal in a previous symbol period; and

generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values.

17. The method of claim 16, wherein a first one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1.

18. The method of claim 16, wherein a second and third of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0.

19. The method of claim 16, wherein a fourth one of said plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1.

20. The method of claim 16, further comprising the step of using said trellis to perform joint equalization and decoding of a signal encoded using said MLT-3 code.

21. The method of claim 16, further comprising the step of concatenating said trellis with a trellis representing a channel to obtain a super trellis.

22. The method of claim 16, wherein said dispersive channel is an Ethernet channel.